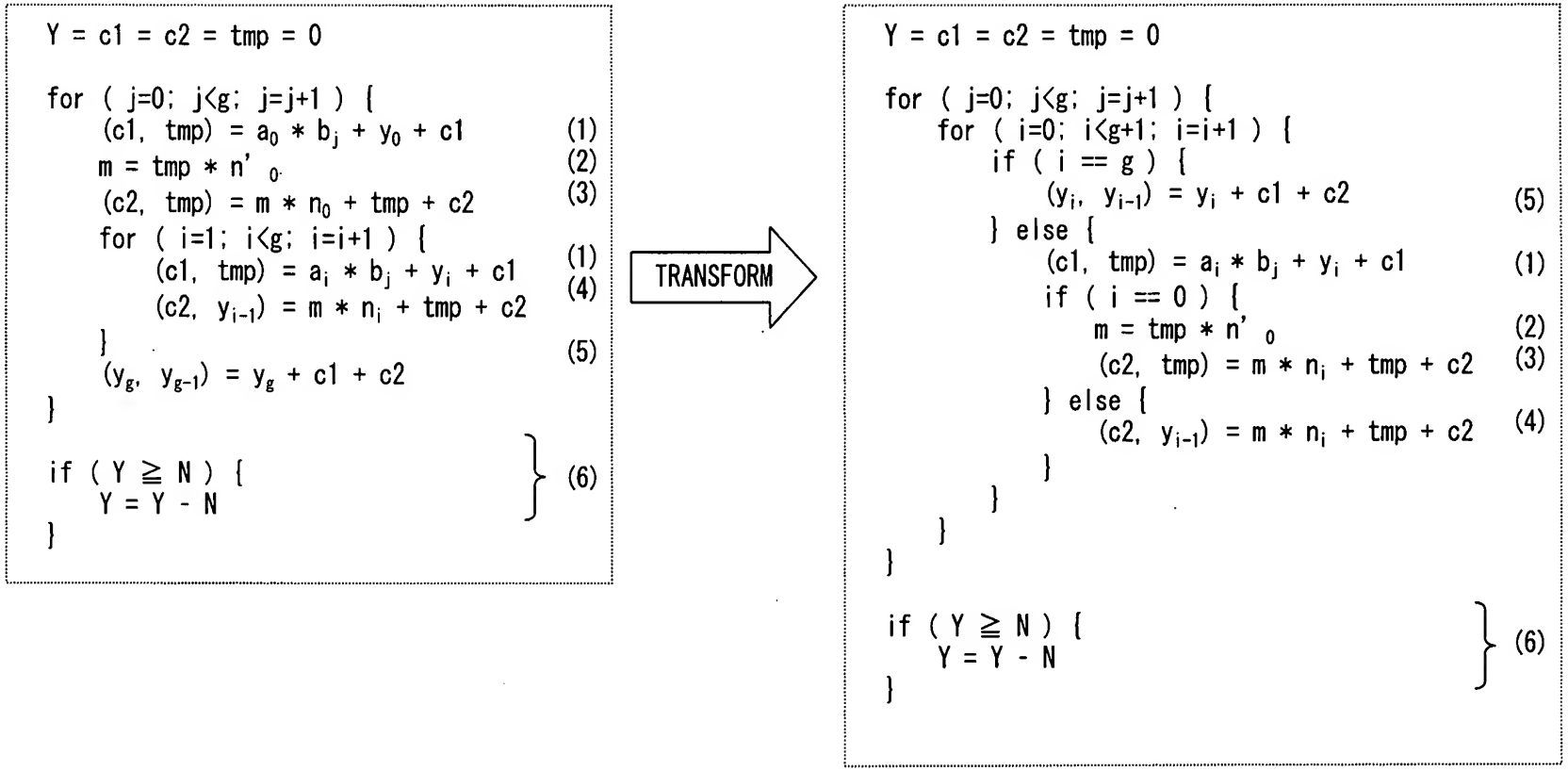

Y = c1 = c2 = tmp = 0
for (j=0; j<g; j=j+1) {
(c1, tmp) = a0 * bj + y0 + c1 (1)
m = tmp * n'0 (2)
(c2, tmp) = m * n0 + tmp + c2 (3)
for (i=1; i<g; i=i+1) {
(c1, tmp) = ai * bj + yi + c1 (1)
(c2, yi-1) = m * ni + tmp + c2 (4)
} (5)
(yg, yg-1) = yg + c1 + c2
}
if (Y ≧ N) { (6)
Y = Y - N
}
TRANSFORM
Y = c1 = c2 = tmp = 0
for (j=0; j<g; j=j+1) {
for (i=0; i<g+1; i=i+1) {
if (i == g) {
(yi, yi-1) = yi + c1 + c2 (5)
} else {
(c1, tmp) = ai * bj + yi + c1 (1)
if (i == 0) {
m = tmp * n'0 (2)
(c2, tmp) = m * ni + tmp + c2 (3)
} else {
(c2, yi-1) = m * ni + tmp + c2 (4)
}
}
}
}
if (Y ≧ N) { (6)
Y = Y - N
}

FIG. 1A

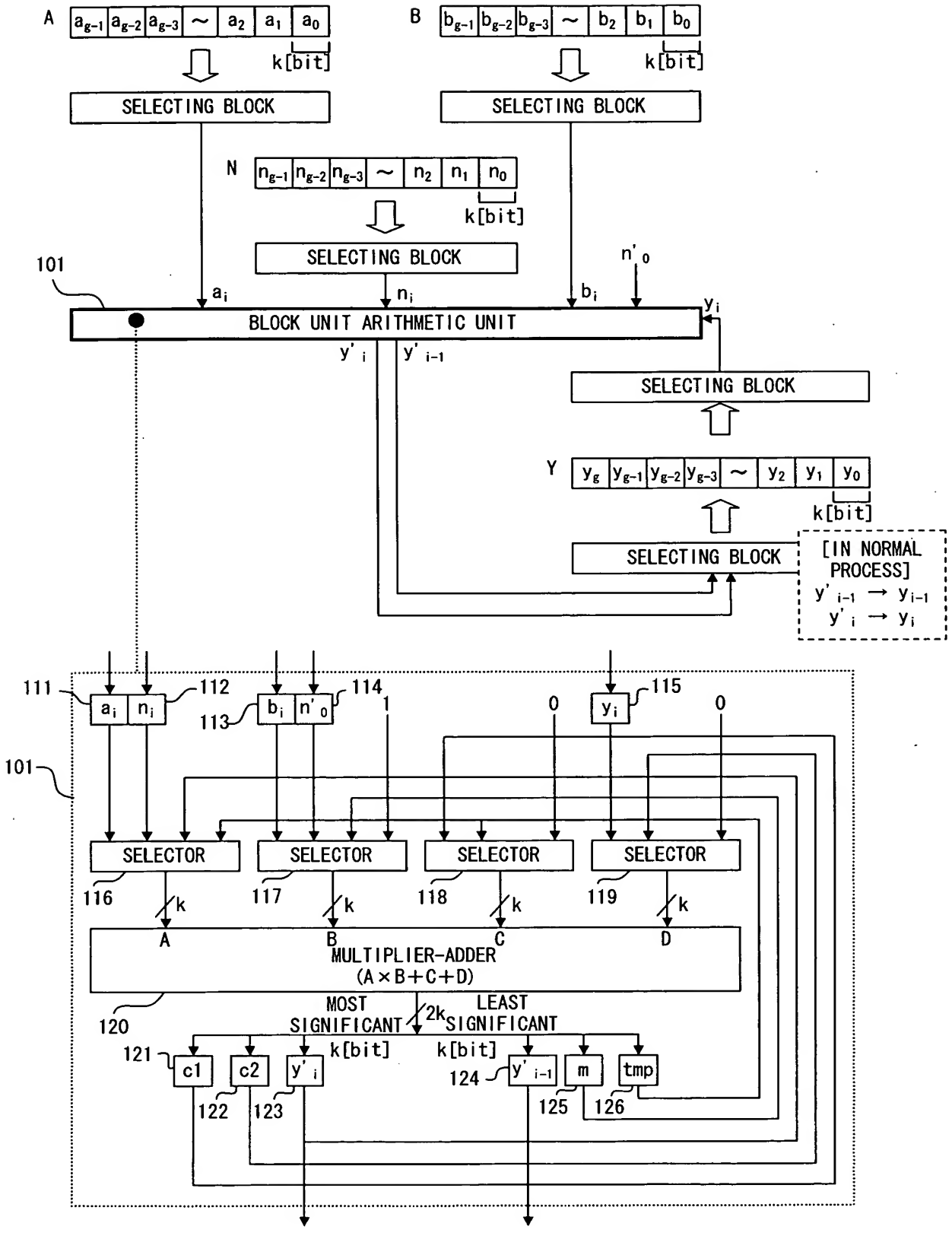

A
B
N
k[bit]
SELECTING BLOCK
101
BLOCK UNIT ARITHMETIC UNIT
Y
[IN NORMAL PROCESS]
111
112
113
114
115
SELECTOR
116
117
118
119
MULTIPLIER-ADDER
(A×B+C+D)
120
MOST SIGNIFICANT
LEAST SIGNIFICANT
121
122
123
124
125
126
c1
c2
m
tmp

FIG. 1B

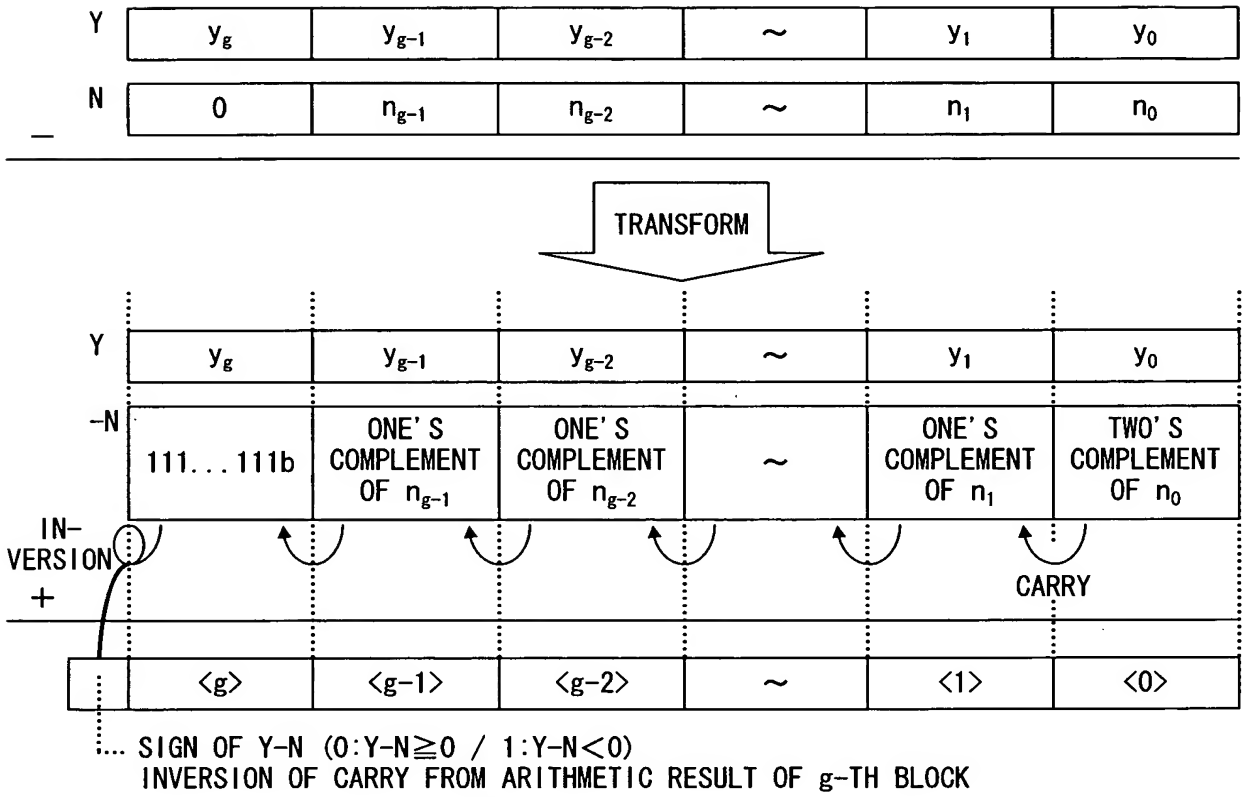

Y
y_g
y_{g-1}
y_{g-2}
~
y_1
y_0
N
0
n_{g-1}
n_{g-2}
~
n_1
n_0
−
TRANSFORM
Y
y_g
y_{g-1}
y_{g-2}
~
y_1
y_0
-N
111...111b
ONE'S COMPLEMENT OF n_{g-1}
ONE'S COMPLEMENT OF n_{g-2}
~
ONE'S COMPLEMENT OF n_1
TWO'S COMPLEMENT OF n_0
IN-VERSION
+
CARRY
<g>
<g-1>
<g-2>
~
<1>
<0>
... SIGN OF Y-N (0:Y-N≧0 / 1:Y-N<0)
INVERSION OF CARRY FROM ARITHMETIC RESULT OF g-TH BLOCK

FIG. 1C

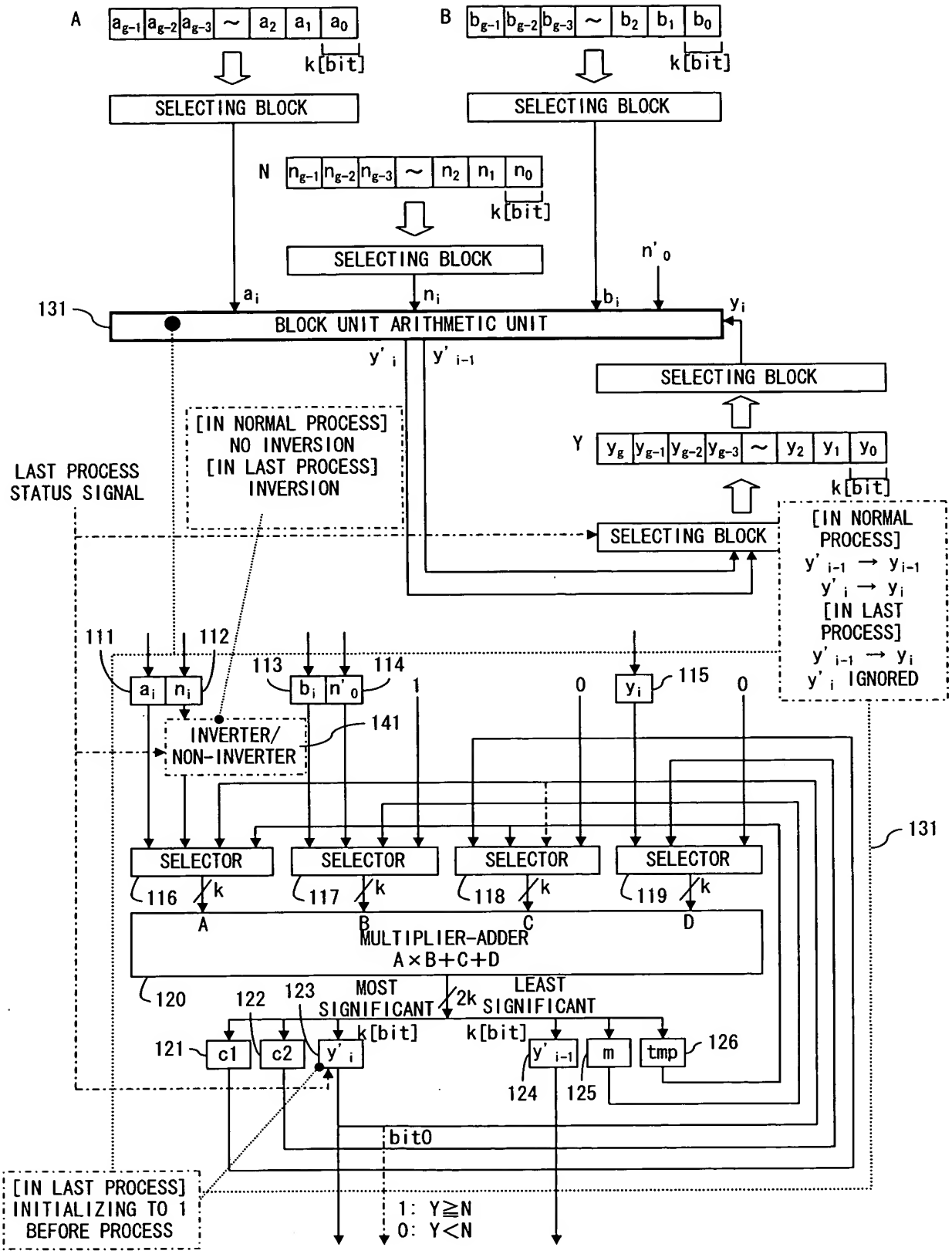

A
B
N
k[bit]
SELECTING BLOCK
131
BLOCK UNIT ARITHMETIC UNIT
Y
[IN NORMAL PROCESS]
NO INVERSION
[IN LAST PROCESS]
INVERSION
LAST PROCESS
STATUS SIGNAL
[IN NORMAL PROCESS]
[IN LAST PROCESS]
IGNORED
INVERTER/
NON-INVERTER
141
SELECTOR
MULTIPLIER-ADDER
A×B+C+D
MOST
SIGNIFICANT
LEAST
SIGNIFICANT
2k
bit0
[IN LAST PROCESS]
INITIALIZING TO 1
BEFORE PROCESS
1: Y≧N
0: Y<N

FIG. 1D

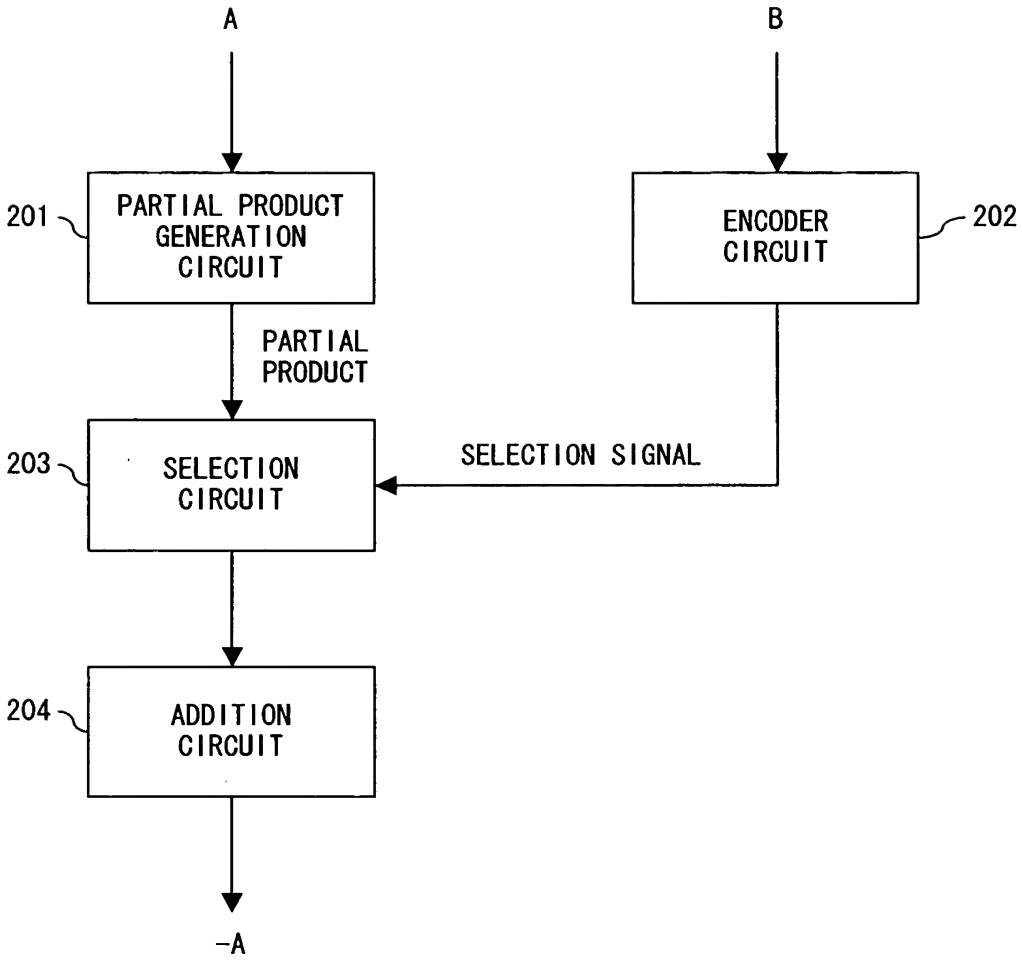

A
B
201
PARTIAL PRODUCT GENERATION CIRCUIT
ENCODER CIRCUIT
202
PARTIAL PRODUCT
203
SELECTION CIRCUIT
SELECTION SIGNAL
204
ADDITION CIRCUIT
-A

FIG. 2A

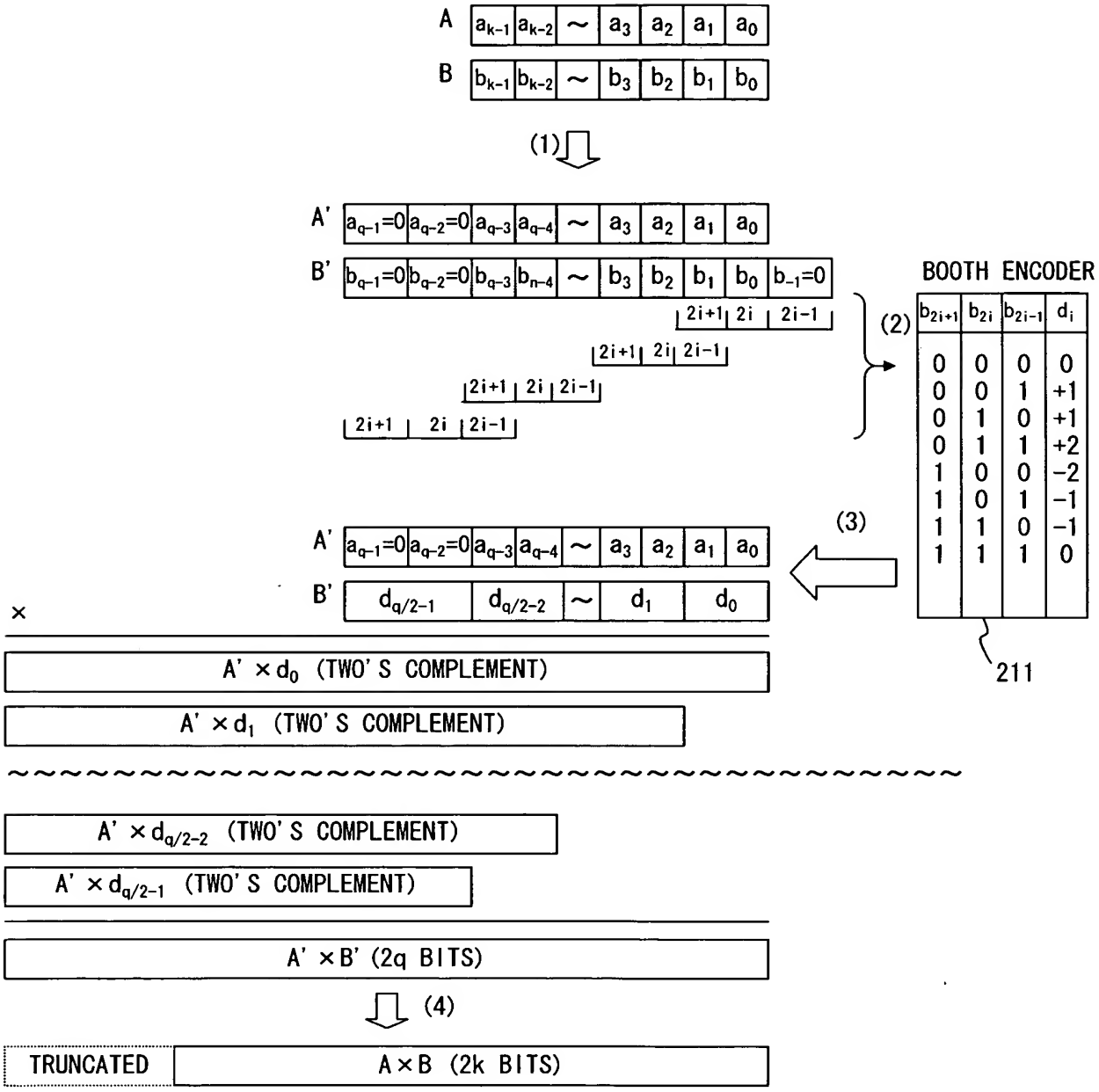
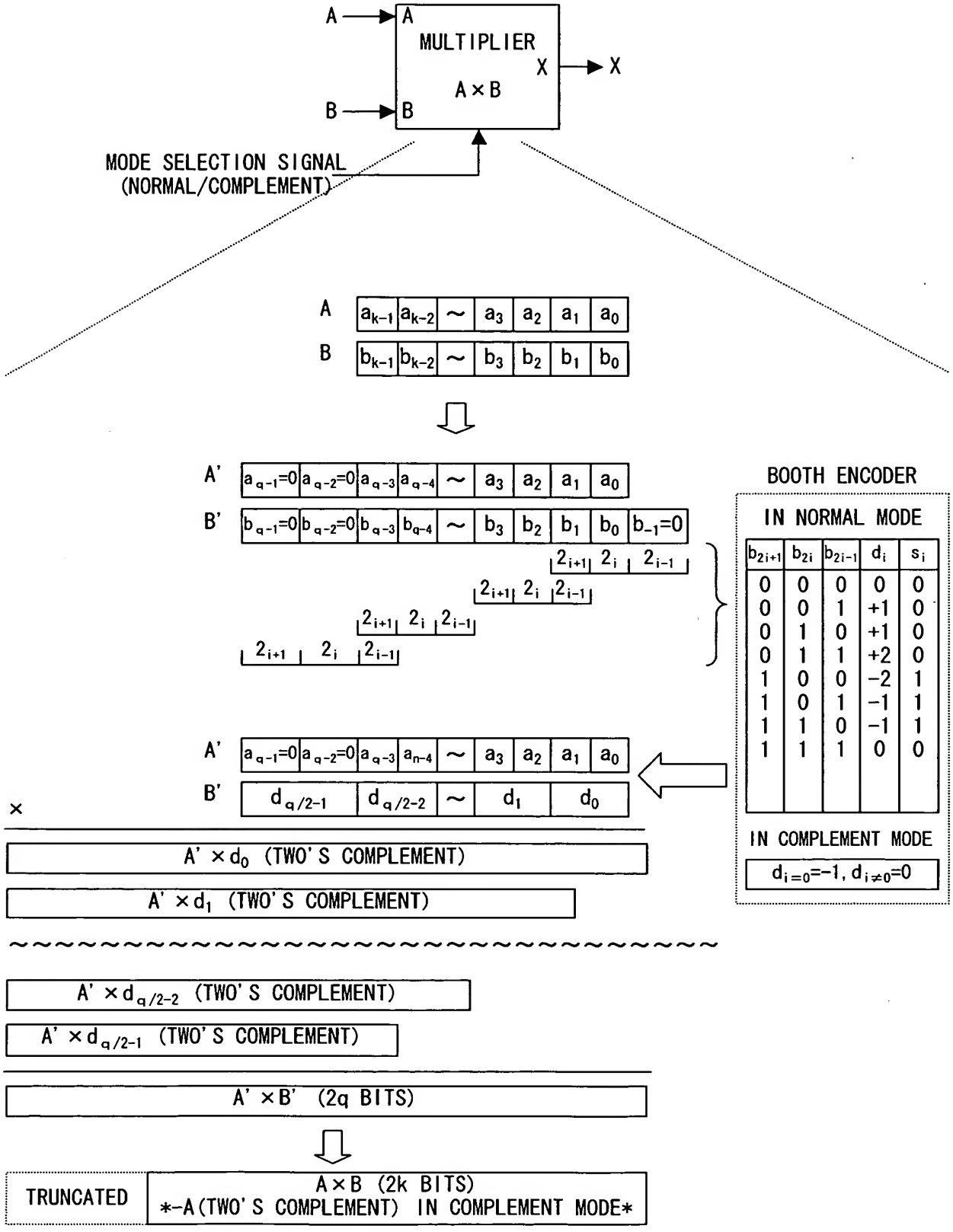
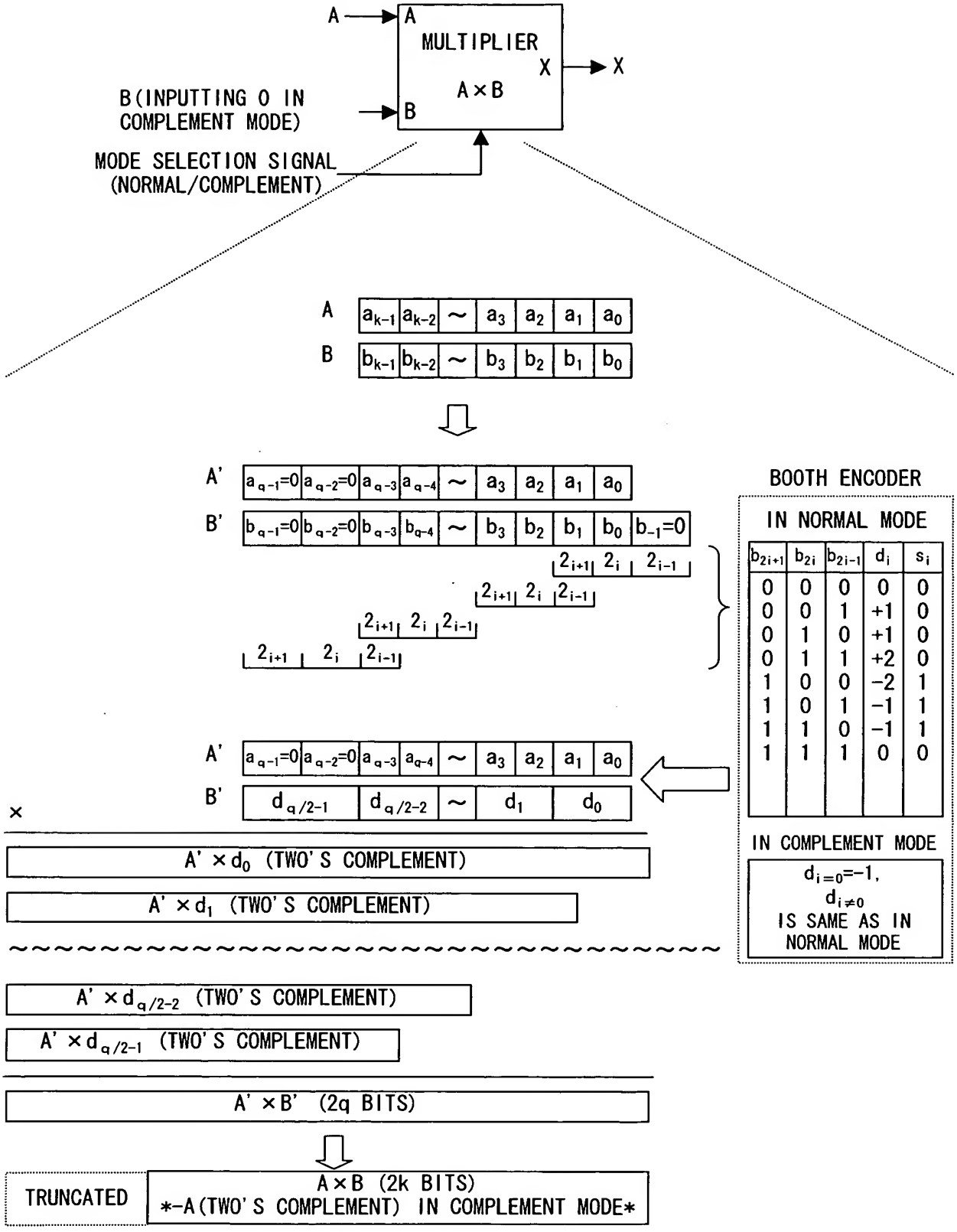

A
a_{k-1} a_{k-2} ~ a_3 a_2 a_1 a_0
B
b_{k-1} b_{k-2} ~ b_3 b_2 b_1 b_0
(1)
A'
a_{q-1}=0 a_{q-2}=0 a_{q-3} a_{q-4} ~ a_3 a_2 a_1 a_0
B'
b_{q-1}=0 b_{q-2}=0 b_{q-3} b_{n-4} ~ b_3 b_2 b_1 b_0 b_{-1}=0
2i+1 2i 2i-1
(2)
BOOTH ENCODER
b_{2i+1} b_{2i} b_{2i-1} d_i
0 0 0 0
0 0 1 +1
0 1 0 +1
0 1 1 +2
1 0 0 −2
1 0 1 −1
1 1 0 −1
1 1 1 0
211
(3)
A'
a_{q-1}=0 a_{q-2}=0 a_{q-3} a_{q-4} ~ a_3 a_2 a_1 a_0
B'
$d_{q/2-1}$ $d_{q/2-2}$ ~ d_1 d_0
×
A' × d_0 (TWO'S COMPLEMENT)
A' × d_1 (TWO'S COMPLEMENT)
A' × $d_{q/2-2}$ (TWO'S COMPLEMENT)
A' × $d_{q/2-1}$ (TWO'S COMPLEMENT)
A' × B' (2q BITS)
(4)
TRUNCATED
A × B (2k BITS)

FIG. 2B



b_{2i+1}	b_{2i}	b_{2i-1}	d_i	s_i
0	0	0	0	0
0	0	1	+1	0
0	1	0	+1	0
0	1	1	+2	0
1	0	0	−2	1
1	0	1	−1	1
1	1	0	−1	1
1	1	1	0	0

FIG. 3



b_{2i+1}	b_{2i}	b_{2i-1}	d_i	s_i
0	0	0	0	0
0	0	1	+1	0
0	1	0	+1	0
0	1	1	+2	0
1	0	0	−2	1
1	0	1	−1	1
1	1	0	−1	1
1	1	1	0	0

FIG. 4

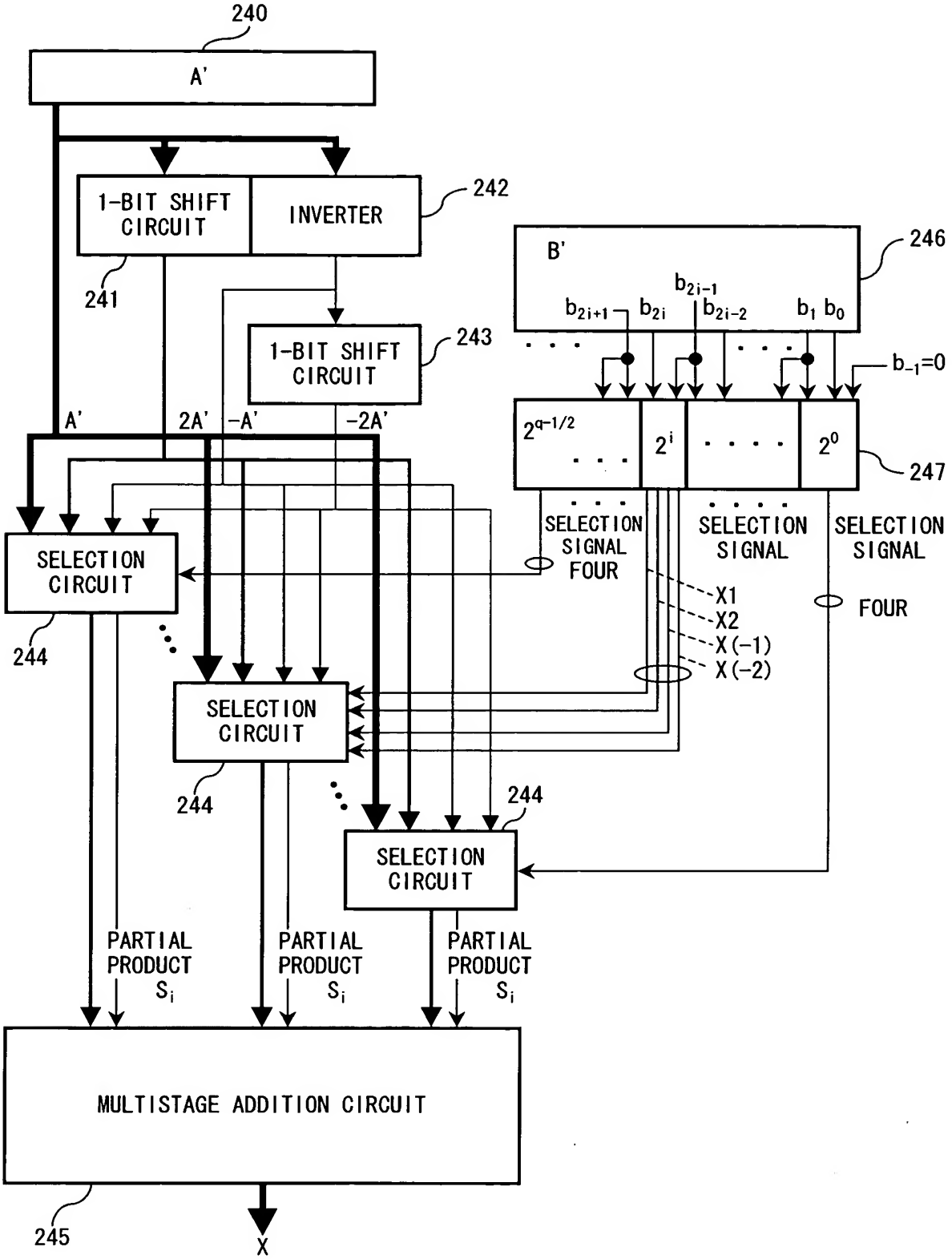

240
A'
1-BIT SHIFT CIRCUIT
INVERTER
242
241
1-BIT SHIFT CIRCUIT
243
B'
246
b_{2i-1}
b_{2i+1} b_{2i} b_{2i-2} b_1 b_0
b_{-1}=0
A'
2A'
-A'
-2A'
$2^{q-1/2}$
2^i
2^0
247
SELECTION SIGNAL FOUR
SELECTION SIGNAL
SELECTION SIGNAL FOUR
SELECTION CIRCUIT
244
X1
X2
X(-1)
X(-2)
SELECTION CIRCUIT
244
244
SELECTION CIRCUIT
PARTIAL PRODUCT S_i
PARTIAL PRODUCT S_i
PARTIAL PRODUCT S_i
MULTISTAGE ADDITION CIRCUIT
245
X

FIG. 5

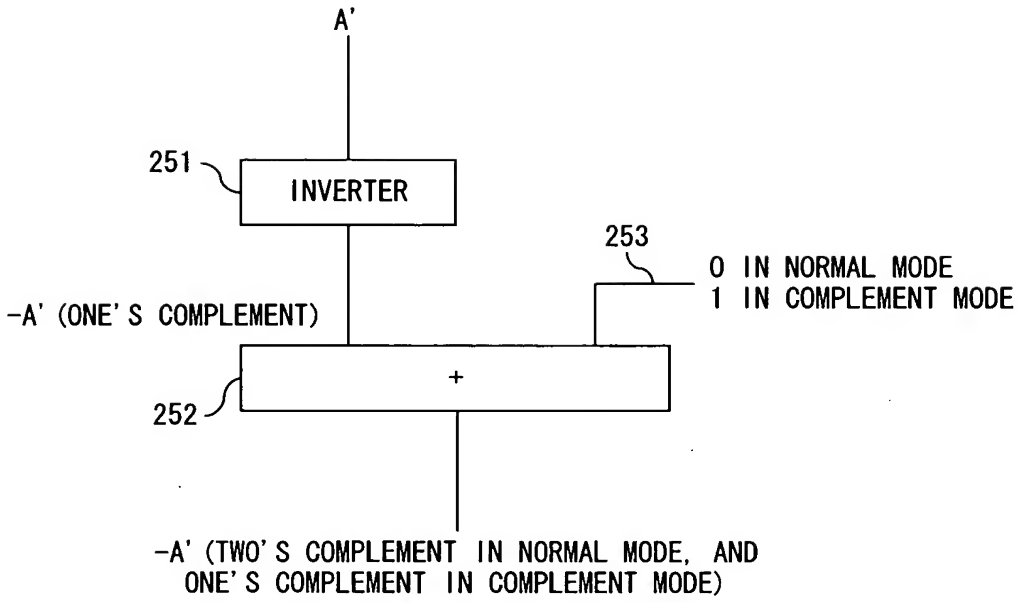

A'
251
INVERTER
253
0 IN NORMAL MODE
1 IN COMPLEMENT MODE
-A' (ONE'S COMPLEMENT)
+
252
-A' (TWO'S COMPLEMENT IN NORMAL MODE, AND
ONE'S COMPLEMENT IN COMPLEMENT MODE)

FIG. 6

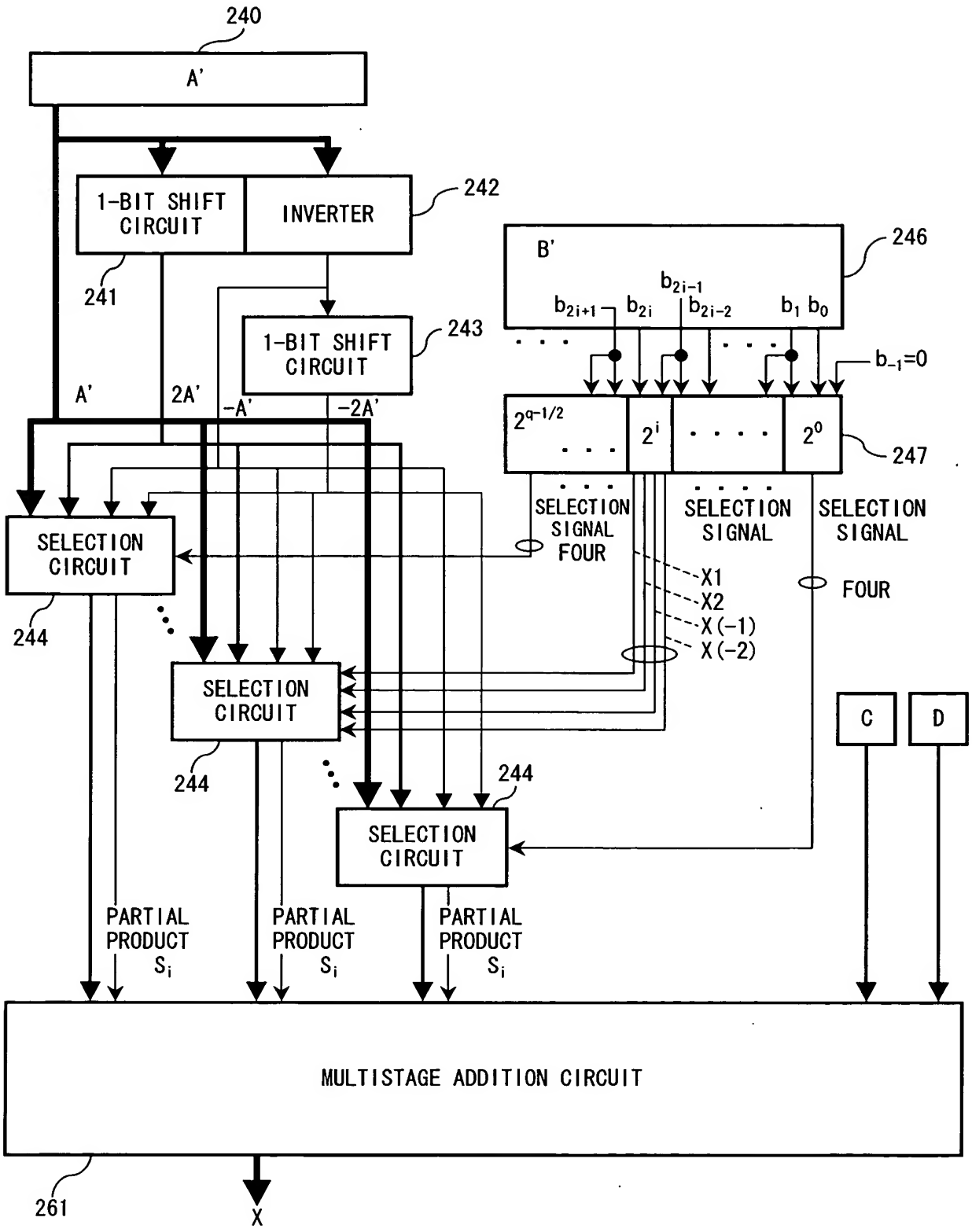

240
A'
1-BIT SHIFT CIRCUIT
INVERTER
242
241
1-BIT SHIFT CIRCUIT
243
B'
246
b_{2i-1}
b_{2i+1}
b_{2i}
b_{2i-2}
b_1 b_0
b_{-1}=0
A'
2A'
-A'
-2A'
$2^{q-1/2}$
2^i
2^0
247
SELECTION SIGNAL FOUR
SELECTION SIGNAL
SELECTION SIGNAL FOUR
SELECTION CIRCUIT
244
X1
X2
X(-1)
X(-2)
SELECTION CIRCUIT
C
D
244
244
SELECTION CIRCUIT
PARTIAL PRODUCT S_i
PARTIAL PRODUCT S_i
PARTIAL PRODUCT S_i
MULTISTAGE ADDITION CIRCUIT
261
X

FIG. 7

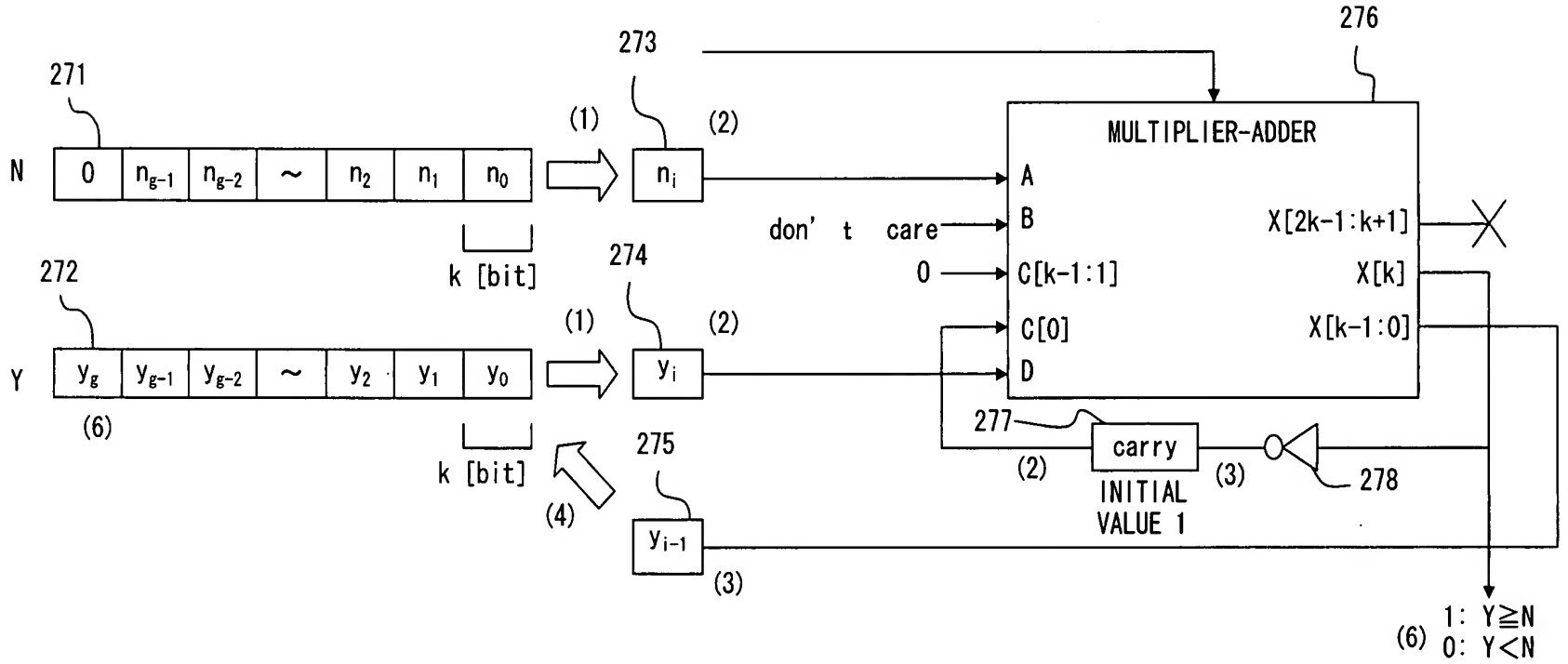

271
273
276
N
0
n_{g-1}
n_{g-2}
~
n_2
n_1
n_0
(1)
(2)
n_i
MULTIPLIER-ADDER
A
B
don' t care
X[2k-1:k+1]
k [bit]
272
274
0
C[k-1:1]
X[k]
(1)
(2)
C[0]
X[k-1:0]
Y
y_g
y_{g-1}
y_{g-2}
~
y_2
y_1
y_0
y_i
D
(6)
277
k [bit]
275
carry
(2)
(3)
278
(4)
INITIAL
VALUE 1
y_{i-1}
(3)
(6) 1: Y≧N
0: Y<N

FIG. 8

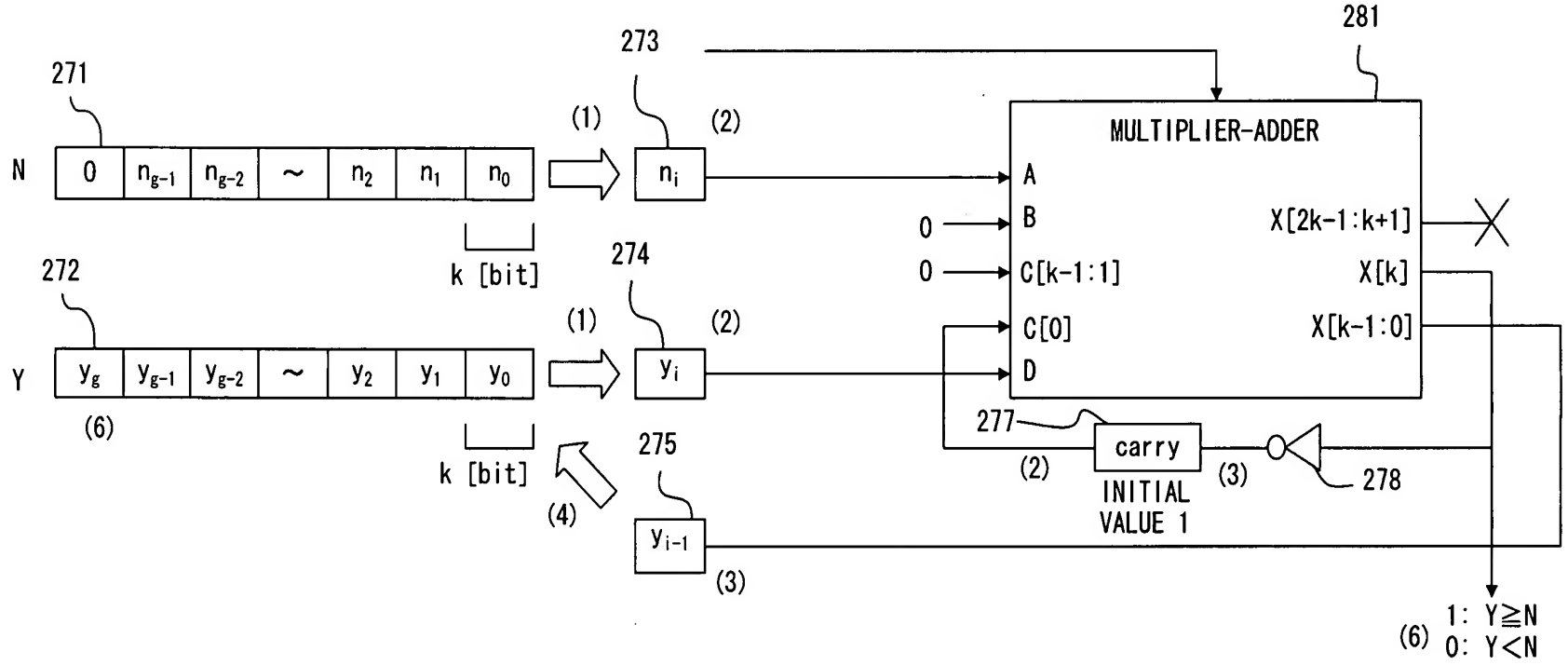

271
273
281
N
0
n_{g-1}
n_{g-2}
~
n_2
n_1
n_0
(1)
(2)
n_i
MULTIPLIER-ADDER
A
B
0
X[2k-1:k+1]
k [bit]
272
274
C[k-1:1]
0
X[k]
Y
y_g
y_{g-1}
y_{g-2}
~
y_2
y_1
y_0
(1)
(2)
y_i
C[0]
X[k-1:0]
D
(6)
277
k [bit]
275
carry
(2)
(3)
278
(4)
INITIAL
VALUE 1
y_{i-1}
(3)
(6)
1: Y≧N
0: Y<N

FIG. 9

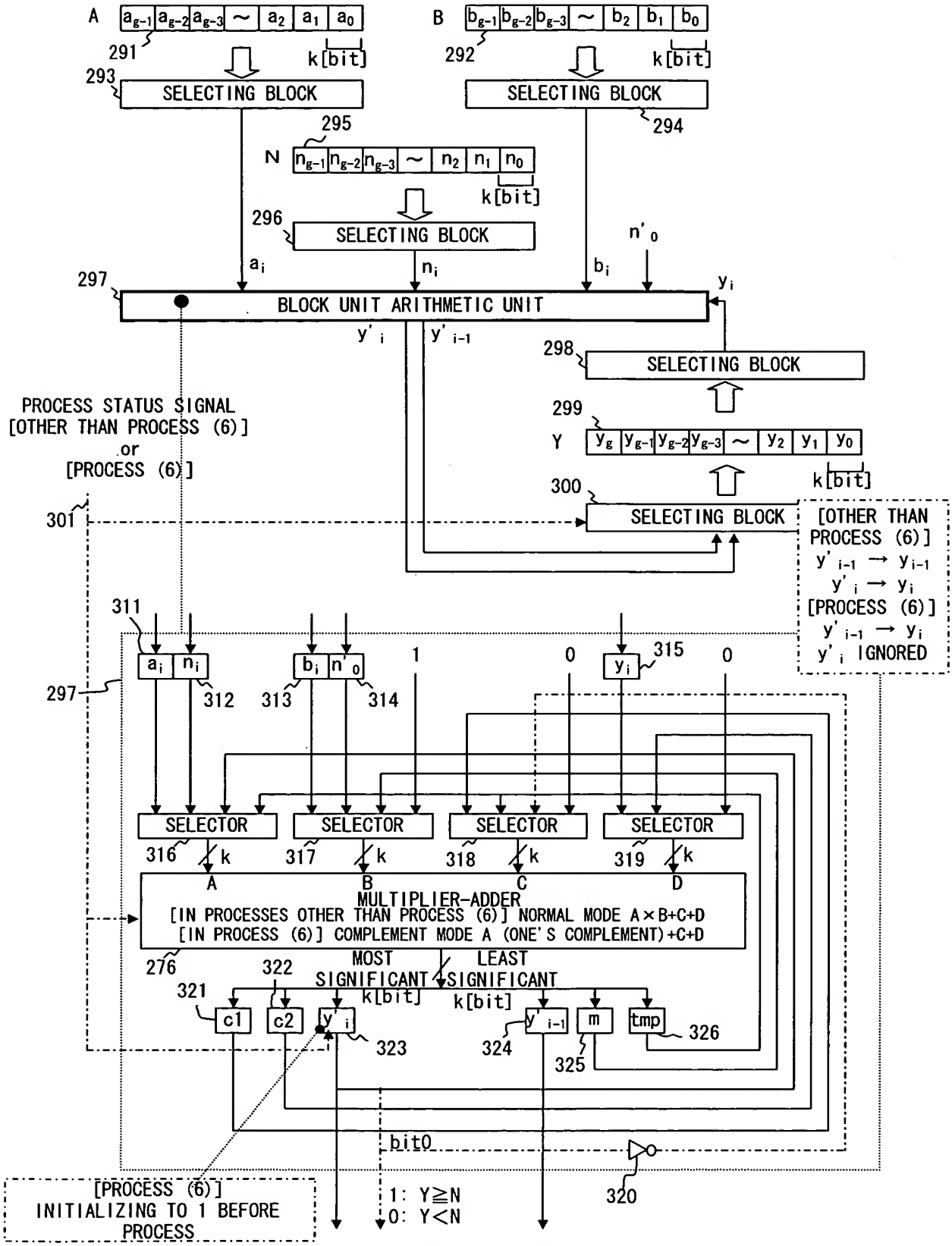

A
B
291
292
k[bit]
293
SELECTING BLOCK
294
295
N
296
297
BLOCK UNIT ARITHMETIC UNIT
298
299
Y
300
301
PROCESS STATUS SIGNAL
[OTHER THAN PROCESS (6)]
or
[PROCESS (6)]
[OTHER THAN PROCESS (6)]
[PROCESS (6)]
y'i IGNORED
311
312
313
314
315
SELECTOR
316
317
318
319
MULTIPLIER-ADDER
[IN PROCESSES OTHER THAN PROCESS (6)] NORMAL MODE A×B+C+D
[IN PROCESS (6)] COMPLEMENT MODE A (ONE'S COMPLEMENT)+C+D
276
MOST SIGNIFICANT k[bit]
LEAST SIGNIFICANT k[bit]
321
322
323
324
325
326
tmp
bit0
320
[PROCESS (6)]
INITIALIZING TO 1 BEFORE PROCESS
1: Y≧N
0: Y<N

FIG. 10

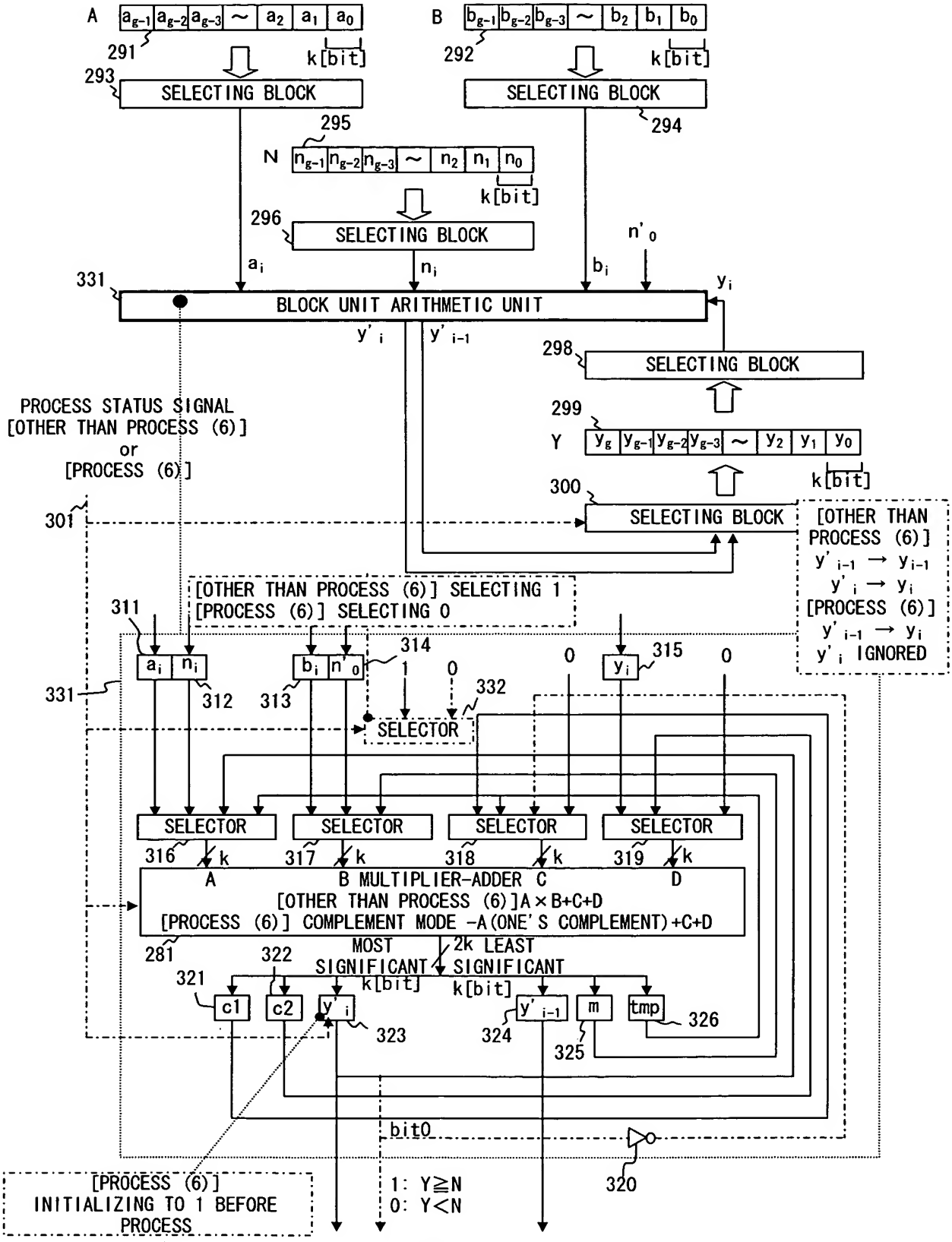

A
B
291
292
k[bit]
293
SELECTING BLOCK
294
295
N
296
331
BLOCK UNIT ARITHMETIC UNIT
298
299
Y
300
301
PROCESS STATUS SIGNAL
[OTHER THAN PROCESS (6)]
or
[PROCESS (6)]
[OTHER THAN PROCESS (6)] SELECTING 1
[PROCESS (6)] SELECTING 0
[OTHER THAN PROCESS (6)]
[PROCESS (6)]
y' i-1 IGNORED
311
312
313
314
315
332
SELECTOR
316
317
318
319
A
B MULTIPLIER-ADDER C
D
[OTHER THAN PROCESS (6)]A×B+C+D
[PROCESS (6)] COMPLEMENT MODE -A(ONE'S COMPLEMENT)+C+D
281
MOST SIGNIFICANT k[bit]
2k LEAST SIGNIFICANT k[bit]
321
322
323
324
325
326
c1
c2
m
tmp
bit0
320
[PROCESS (6)]
INITIALIZING TO 1 BEFORE PROCESS
1: Y≧N
0: Y<N

FIG. 11